

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
11 August 2005 (11.08.2005)

PCT

(10) International Publication Number
WO 2005/073792 A1

(51) International Patent Classification⁷: **G02F 1/1362**

(21) International Application Number:

PCT/IB2004/052796

(22) International Filing Date:

14 December 2004 (14.12.2004)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

PCT/IB2004/000065

5 January 2004 (05.01.2004) IB

(74) Agents: TSUGARU, Susumu et al.; c/o Philips Japan, Ltd., Philips Bldg., 2-13-37, Kohnan, Minato-ku, Tokyo 108-8507 (JP).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(71) Applicant (*for all designated States except US*): KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

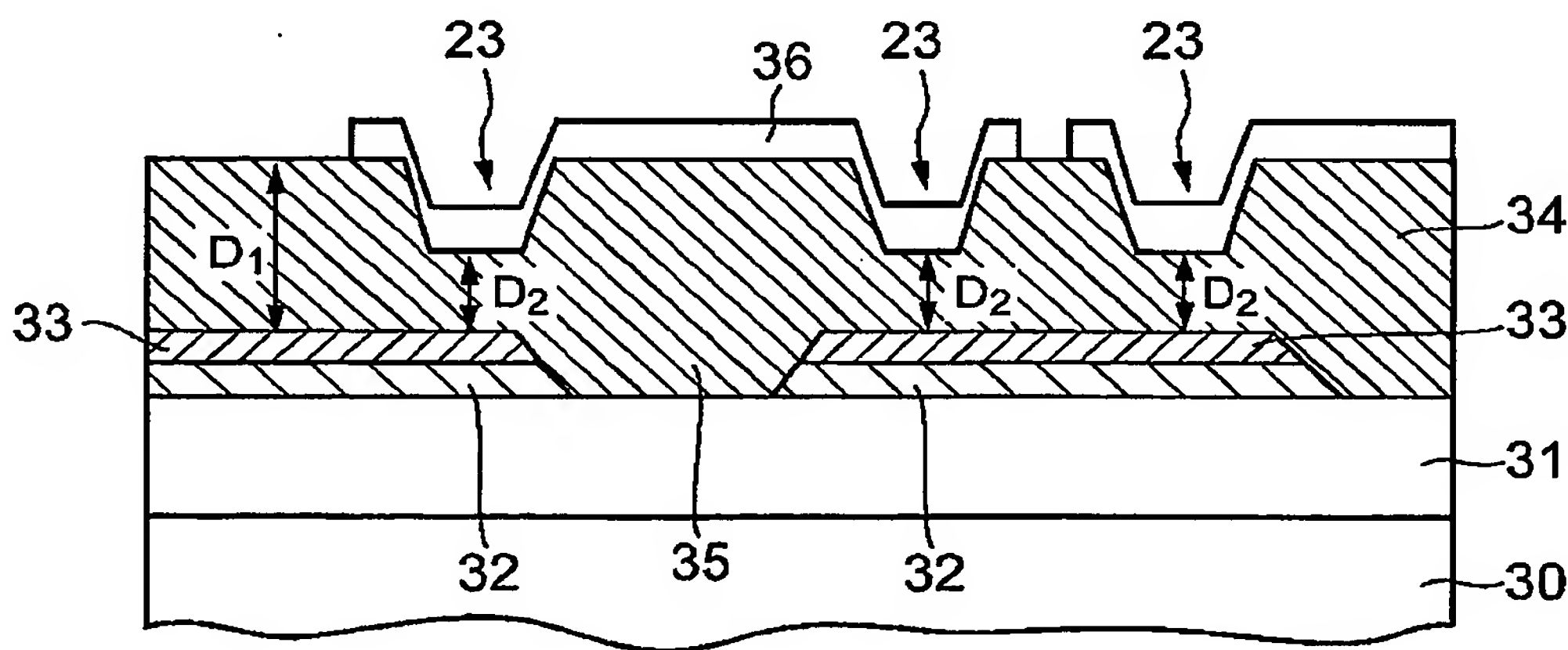
(72) Inventor; and

(75) Inventor/Applicant (*for US only*): TANAKA, Hideo [JP/JP]; c/o Philips Japan, Ltd., Philips Bldg., 2-13-37 Kohnan, Minato-ku, Tokyo 108-8507 (JP).

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: LIQUID CRYSTAL DISPLAY DEVICE HAVING ESD PROTECTION CIRCUIT AND METHOD FOR MANUFACTURING THE SAME



(57) Abstract: A source electrode and a drain electrode on a silicon oxide film (31) each has a double-layered structure of an ITO film (32), a transparent electrode, and a metal film (33) formed on the ITO film (32). A gap (35), no source electrode and drain electrode region, is formed between the source electrode and the drain electrode. A silicon nitride film (34) (a gate insulating film) is formed on the source electrode and the drain electrode and in the gap (35). The silicon nitride film (34) is a first region D₁ having a relatively large thickness and a second region D₂ having a relatively small thickness. The region D₂ of the silicon nitride film (34) is provided with an MIM structure. A gate bus layer (36) is formed on the silicon nitride film (34). An MIM structure is formed in the second region D₂.



Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.